CLAIMS:

1. A memory device comprising, in a single integrated circuit package:
- a static memory means (10, 12) defining at least first and second nodes (A, B) communicatively connected with read and/or write data lines; and
- at least one non-volatile memory means (14, 16) associated with said static memory means (10, 12), and writing data stored therein to said static memory means (10, 12); characterized in that said non-volatile memory means comprises at least two non-volatile memory elements (14, 16) cross-coupled to said first and second nodes (A, B) respectively.

2. A memory device according to claim 1, wherein said non-volatile memory elements (14, 16) comprise embedded flash or EEPROM elements.

3. A memory device according to claim 1 or 2, wherein said non-volatile memory elements (14, 16) comprise double or single poly floating gate type memory cells.

4. A memory device according to claim 1, wherein said non-volatile memory elements (14, 16) comprise devices which can be programmed and erased by means of tunneling of charges.

5. A memory device according to any one of claims 1 to 4, wherein the cross-coupled non-volatile memory elements (14, 16) are programmed with opposite data.

6. A memory device according to any one of claims 1 to 5, wherein the static memory means comprises a pair of cross-coupled inverters (10, 12).

7. A memory device according to any one of claims 1 to 6, wherein a first non-volatile element (14) has a control gate connected to a first node (B) and a source connected to a second node (A), and a second non-volatile element (16) has a control gate connected to the second node (A) and a source connected to the first node (B).

8. A memory device according to claim 7, wherein the drain of each non-volatile element (14, 16) is connected by means of a respective transistor (18, 20), to a supply means (VDP).

9. A memory device according to any one of claims 1 to 8, wherein one or more respective selection transistors (22) are provided, by means of which the nodes (A, B) are communicatively coupled to the read and/or write lines.

10. A memory device according to any one of claims 1 to 9, including one or more isolation transistors (24).

11. A reconfigurable programmable logic device including a memory device according to any one of claims 1 to 10.

12. A field programmable gate array including a memory device according to any one of claims 1 to 11.